IN THE CLAIMS

Kindly cancel claims 2 and 3, without prejudice, and amend claims 1, 4 and 11 as shown in the following claim listing:

1.(currently amended) A processing apparatus for implementing a systolic-array-like structure, said apparatus comprising:

a) input means for inputting data;

b) register means for storing said input data in a predetermined sequence;

c) processing means for processing data received from said register means based on control signals generated from instruction data; and

d) register control means for controlling the depth of said register means in accordance with said instruction data; wherein said register means comprises distributed register files provided at input terminals of a plurality of functional units of said processing means; and wherein said distributed register files comprise depth-configurable FIFO register files addressable for individual registers.

2. (cancel)

3. (cancel)

4.(currently amended) An apparatus according to claim ~~3~~ 1, wherein said register control means are arranged to determine the last logical register of said FIFO register files based on control signals derived from said instruction data.

5.(previously presented) An apparatus according to claim 1, further comprising at least one issue slot for storing said instruction data.

6. (original) An apparatus according to claim 5, wherein said register control means are arranged to use a part of the bit pattern of said instruction data stored in said at least one issue slot for controlling said depth of said register means.

7.(previously presented) An apparatus according to claim 1, wherein said programmable processing apparatus is a scalable VLIW processor or a coarse-grained reconfigurable processor.

8.(previously presented) An apparatus according to claim 1, wherein said distributed register files are connected to an interconnect network made up of a plurality of point-to-point connection lines.

9.(original) An apparatus according to claim 8, wherein said point-to-point interconnect lines have a single source.

10.(original) An apparatus according to claim 8, wherein said interconnect network is partially connected.

11.(currently amended) A processing method for implementing a systolic-array-like structure, said method comprising:

a) storing ~~said~~ input data in a register file in predetermined sequence;

b) processing data received from said register file based on control signals generated from instruction data; ~~and~~

c) controlling the depth of said register file in accordance with said instruction data~~.~~ ;

d) providing said register file with distributed register files at input terminals of a plurality of functional units; and

e) providing said distributed register files with depth-configurable FIFO register files addressable for individual registers.